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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/625,567	07/24/2003	Jun Funakoshi	108066-00091	1074

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EXAMINER

TRAN, NHAN T

ART UNIT	PAPER NUMBER
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2622

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/20/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/625,567	FUNAKOSHI ET AL.	
	Examiner	Art Unit	
	Nhan T. Tran	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 24 July 2003 and 08 February 2007.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) 3-6, 12, 14, 16/3-16/6, 16/12, 16/14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1, 2, 9-11, 16/1, 16/2, 16/9-16/11 is/are rejected.
- 7) ☒ Claim(s) 7, 8, 13, 15, 16/7, 16/8, 16/13 & 16/15 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 24 July 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____

DETAILED ACTION

Election/Restrictions

1. Applicant's election without traverse of Species IV, Figure 13 corresponding to claims 1, 2, 7-11, 13, 15 & 16 in the reply filed on 2/8/2007 is acknowledged. It is noted that claim 16 contains multiple incorporated limitations of "the image processing circuit according to any of claim 1 to claim 15", and therefore only limitations of claims 1, 2, 7-11, 13 and 15 are considered as the multiple incorporated limitations of claim 16 (numbered as 16/1, 16/2, 16/7-16/11 and 16/15).

According to the election, claims 3-6, 12, 14, 16/3-16/6, 16/12 and 16/14 are withdrawn from consideration.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 7/24/2003 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

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4. Claim 1 is objected to because of the following informalities: claim recites "wherein said predetermined offset includes, a first offset which is set according to each color..." The **comma** (,) in front of "a first offset" should be removed to complete a sentence. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim 9 is rejected under 35 U.S.C. 102(e) as being anticipated by Koren et al. (US 6,831,686 B1).

Regarding claim 9, Koren discloses an image processing circuit (Figs. 1 & 2), comprising: a correction circuit (Fig. 2) for or adding or subtracting an offset ($\alpha(i)$) for each column (by summer S1), which is set according to a plurality of columns (a plurality of columns of image sensor shown in Fig. 3), to or from pixel signals obtained for each column by amplifying photoelectric conversion signals of pixels, said pixels having photoelectric conversion elements and being arranged in column and row

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directions (see col. 3, line 4 – col. 4, line 3 and it should be noted that each offset is derived from a plurality of columns of at least one line shown in Fig. 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 1, 10, 16/1 & 16/10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren et al. (US 6,831,686 B1) in view of Park (US 2003/0202111 A1).

Regarding claim 1, Koren discloses an image processing circuit (Figs. 1 & 2), comprising:

a sensitivity correction circuit which adds or subtracts (by summer S1) a predetermined offset ($\alpha(i)$) to or from a pixel signal obtained, for each column, by amplifying photoelectric conversion signals of pixels, and multiplies the result by a predetermined gain ($1/\beta(I, j)$), said pixels having a photoelectric conversion element (photodiode) respectively and being arranged in column and row directions (Figs. 1-3), wherein said predetermined offset includes an offset ($\alpha(i)$) which is set according to a plurality of columns (see col. 3, line 4 – col. 4, line 3 and it should be noted that each offset is derived from a plurality of columns of at least one line shown in Fig. 3).

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Koren teaches a sensitivity correction circuit for an imaging apparatus as analyzed above but Koren is silent about that the sensitivity correction circuit is a color sensitivity correction circuit and the predetermined offset includes a first offset which is set according to each color.

However, as taught by Park, a color sensitivity correction circuit is disclosed, wherein an offset is set according to each color (e.g., Red offset, Green offset, Blue offset shown in Fig. 6) so that image quality is improved with proper luminance (see Park, paragraphs [0029]-[0030] and [0004]).

Therefore, it would have been obvious to one of ordinary skill in the art to modify the image processing circuit in Koren for correcting color sensitivity by setting an offset to the circuit according to each color so as to improve image quality with proper luminance as suggested by Park.

Regarding claim 10, Koren in view of Park also discloses all limitations of claim 10 as analyzed in claim 1 and Fig. 6 of Park, wherein each color is multiplied by a gain value.

Regarding claims 16/1 & 16/10, Koren in view of Park discloses a color image sensor and the image processing circuit as analyzed in claim 1. Additionally, the combination of Koren and Park also discloses a pixel array where said pixels are arranged in column and row directions (see Fig. 3 in Koren and Fig. 1 in Park); and a column output circuit which is disposed for each column, amplifies (by operational

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amplifier) the photoelectric conversion signals of said pixels arranged in the column direction; and outputs said image signals (see Koren, Fig. 1, col. 3, lines 11-13).

7. Claims 2, 11, 16/2, 16/11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koren et al. (US 6,831,686 B1) and Park (US 2003/0202111 A1) and in further view of Chiu (US 2003/0016294 A1).

Regarding claim 2, as analyzed in claim 1 above, the combined teachings of Koren and Park disclose the color sensitivity correction circuit comprises a first offset and a second offset that are stored in a memory (RAM in Fig. 2 of Koren or register in Fig. 6 of Park) and output to add or subtract from the pixel signals. Koren and Park are silent about the first offset and second offset are stored in a table.

It is well recognized in the art that offsets for image correction can be stored in table format (i.e., a look-up table) so as to provide a compensation apparatus with less storage space and faster accessing speed as suggested by Chiu in Fig. 2 and paragraphs [0005] & [0022].

Therefore, it would have been obvious to one of ordinary skill in the art to store the first and second offsets of the apparatus of Koren and Park in a table so as to provide a compensation apparatus with less storage space and faster accessing speed as suggested by Chiu above.

Regarding claim 11, the limitations of claim 11 are also met by the analysis of claim 2.

Regarding claims 16/2 & 16/11, see the analyses of claims 2 and 16/1 above.

Allowable Subject Matter

8. Claims 7, 8, 13, 15, 16/7, 16/8, 16/13 & 16/15 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

The prior art of record fails to teach or fairly suggest the limitations of said color sensitivity correction circuit further comprises an offset generation section which compares pixel signals for each column with a reference value corresponding to brightness of at least one frame of an image, and dynamically generates the second offset according to the result of the comparison.

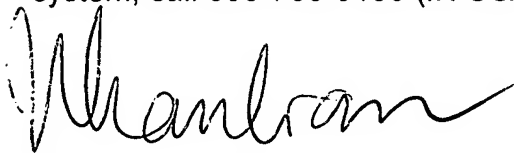
Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Friday, 8:00am - 4:30pm.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

A handwritten signature in black ink, appearing to read 'Nhan Tran', with a stylized, flowing script.

NHAN T. TRAN
Patent Examiner